What is claimed is:

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1. A unicast/multicast system, comprising:

an internal cell generating section that generates an internal cell based on user data;

an internal cell receiving section that outputs the internal cell to a timing generating section and outputs a header field of the internal cell to an index search section;

an output port conversion table that stores the relation of output index information and output port number in the form of one-to-one for the unicast and one-to-multiple for the multicast;

said index search section that extracts output index information from the header field to be sent from said internal cell receiving section, refers to said output port conversion table for an output port number corresponding to the output index information extracted, and outputs the output port number obtained from said output port conversion table to a destination-based distribution section;

said destination-based distribution section that controls a gate section based on the output port number input from said index search section;

a timing generating section that delays the internal cell input from said internal cell receiving section and then outputs it said gate section;

said gate section that distributes the internal cell input from said timing generating section to said gate section according to the control of said destination-based distribution section;

a plurality of buffers that each store the internal cell distributed from said gate section and, when receiving the internal

cell distributed from said gate section, sends switching request signal to a switching request adjusting section;

said switching request adjusting section that adjusts the switching request signal input from said buffers between said buffers and determines a route in a crosspoint switch; and

said crosspoint switch that outputs the internal cell stored in said buffers through the route determined by said switching request adjusting section.

2. A unicast/multicast system, according to claim 1, wherein:

said output port conversion table is a memory to an address of which the output index information is assigned, data stored in the address being represented as a bit pattern and corresponding to an output port number.

3. A unicast/multicast system, according to claim 1, wherein:

said buffers have buffers for the unicast and buffers for the multicast assigned to one output port number;

said header section has a unicast/multicast identifier in addition to the output index information;

said destination-based distribution section controls said gate section based on the unicast/multicast identifier as well as the output index information; and

said gate section distributes the internal cell input from said timing generating section to the unicast buffer or multicast buffer designated by said destination-based distribution section.

4. A unicast/multicast system, according to claim 3, further comprising:

a buffer management section that, if there is stored an internal cell in the multicast buffer when the transfer allowance is issued from said crosspoint switch, transfers, by priority, the internal cell in the multicast buffer to the crosspoint switch.

5. A unicast/multicast system, according to claim 1, wherein:
said user data is of IP packet or ATM cell.

6. A unicast/multicast system, according to claim 1, wherein:
said buffers each are of a FIFO type buffer.

7. A unicast/multicast system, comprising:
an internal cell generating section that generates an internal cell to include its output index information based on user data; and
an output port conversion table that stores the relation of the output index information and an output port number for the internal cell in the form of one-to-one for the unicast and one-to-multiple for the multicast.

8. A unicast/multicast system, according to claim 7, wherein:
said output port conversion table is a memory to an address of which the output index information is assigned, data stored in the address being represented as a bit pattern and corresponding to an output port number.

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